

IMP-ARIO / IMP-ARIO64 Hardware User Manual

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<http://www.epcio.com.tw>

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Chapter 1 Overview

The Asynchronous Remote I/O Board (IMP-ARIO), a product developed by the MSL of ITRI, is a remote I/O board for dedicated digital communications format. There are two models of the asynchronous remote I/O board depending on the inputs and outputs, which are IMP-ARIO and IMP-ARIO64. It is mainly used for the input/output control in general industrial machines.

1.1 Hardware Specifications

Item	Spec.	
	IMP-ARIO	IMP-ARIO64
Communications Interface	Asynchronous Serial	
Topological Structure	Serial Connection	
Operating Temperature	0°C – 55°C	
Dimension	130mm x 140mm	178mm x 108mm
Power Requirement	5V/550mA	5V/1000mA
Maximum Refresh Rate	20μsec/32 channels	40μsec/64 channels
Input	16	32
Output	16	32
Maximum Input/Output	512 Inputs / 512 Outputs	
Maximum Output Current at a Single Output	100mA	
Inputs (PhotoCouple)/ Outputs (PhotoMosRelay)	Source Type: COM voltage at 5 – 24V	
	Sink Type: COM voltage at 0V	

1.2 System Connection

The IMP-ARIO/IMP-ARIO64 is a master-slave input/output control system. The IMP-2 (master) carries out the data transmission and reception using the serial transmission with the IMP-ARIO/IMP-ARIO64 (slave) through the serial transmission format. With the remote wiring-saving design as well as the dedicated digital communications format, it can connect up to 512 inputs and 512 outputs in a system at the same time. With each IMP-ARIO has 16 inputs and 16 outputs, and each IMP-ARIO64 has 32 inputs and 32 outputs. The system can support up to 512 inputs and 512 outputs, i.e., a control system with up to 1024 I/O channels. Such a remote I/O board concept can significantly reduce the wiring complexity, which translates to not only cost reduction, but also improved reliability and easy maintenance of the system.

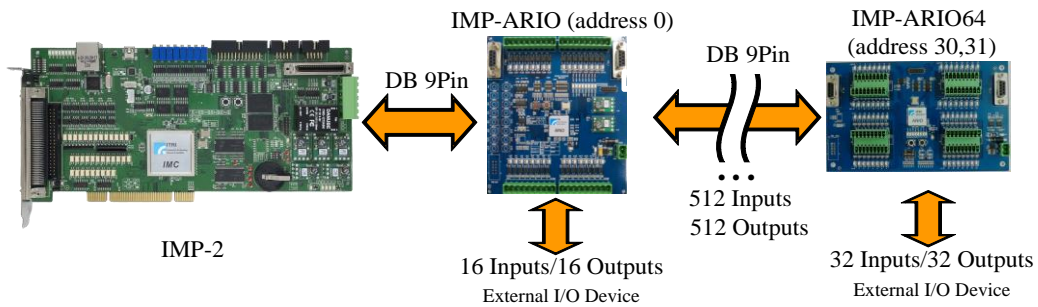


Fig. 1-1 The IMP-2 master-slave control system connection diagram

Fig. 1-1 shows the system connection diagram of the IMP-2. The IMP-2 carries out the data access with the IMP-ARIO/IMP-ARIO64 through the DB 9-Pin cable for reading the inputs and controlling the outputs.

1.3 Description of Functions

Fig. 1-2 shows the block diagram of the transmission function of the IMP-2 remote I/O. The **IMC (Master)** is in charge of reading and refreshing the status of the remote I/O within the cycle period. The output signals are first converted into differential signal format through the **output driving circuits** and then transmitted to **ARIO (Slave)** through the **DB 9-Pin** cable; the input signals are received from the signals transmitted by the **ARIO (Slave)** through the **DB 9-Pin** cable and then transmitted to the **IMC** after being **isolated** by the **photo coupler**.

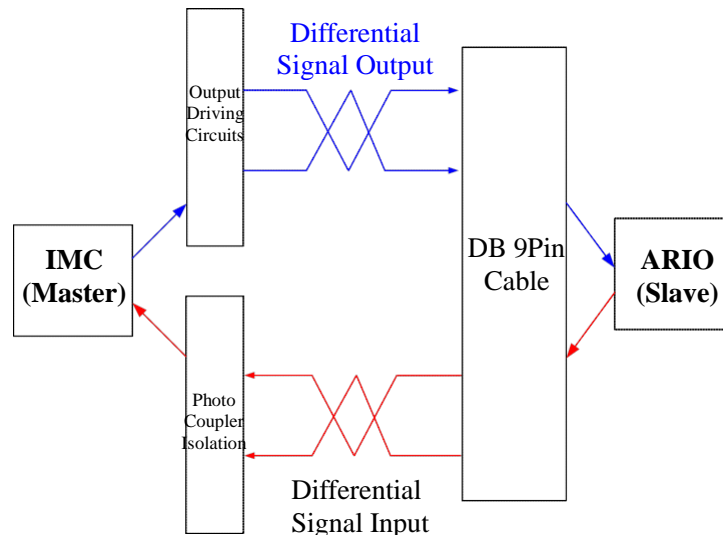


Fig. 1-2 The transmission function of IMP-2 Remote I/O

Fig. 1-3 shows the functional block diagram of the ARIO. The *ARIO (Slave)* is in charge of receiving the differential signals from IMP-2 within the period through the *TR_1*, and then signals are decoded after being **isolated** by the **photo couplers**. The decoded signals are then sent to the **output** through the **PhotoMOS relay**. For the input, the input signals are received at the **input** and then sent to the *ARIO (Slave)* for encoding after being isolated by the **photo couplers**. The encoded signals are then relayed by the **output driving circuit** and sent back to IMP-2 through the *TR_1*. The *TR_2* can then connect with the *TR_1* of the next card, and the dotted line shows the connection status.

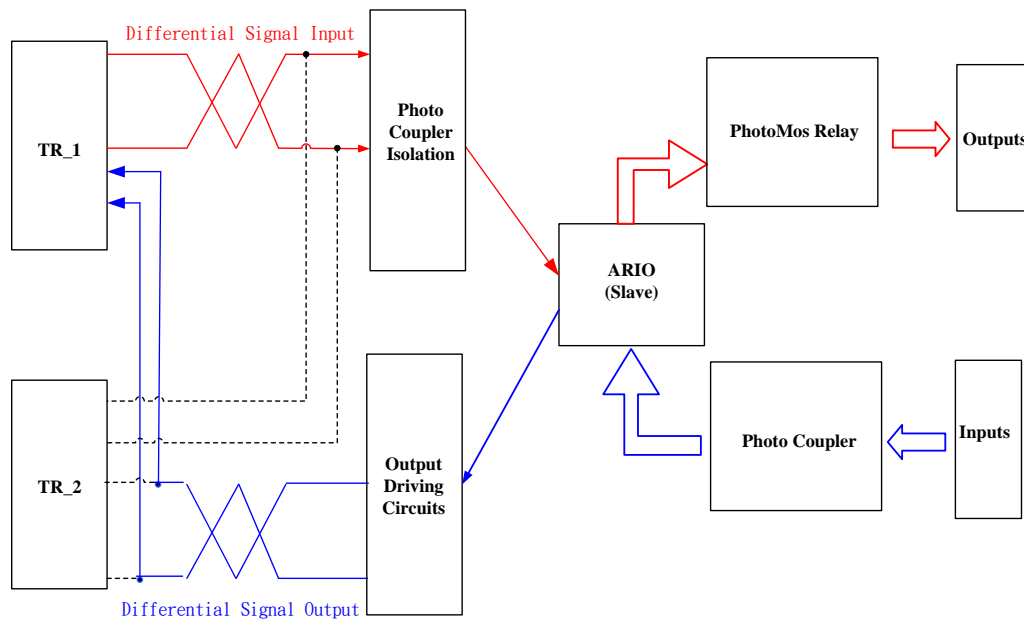


Fig. 1-3 Functional block diagram of ARIO

1.4 Description of Wiring

The connection between the IMP-2 and the IMP-ARIO/IMP-ARIO64 is shown in Fig. 1-4. One terminal of the ribbon cable on the PCI bracket is connected with a 10-Pin female socket which matches the 10-Pin male plug on the RIO of IMP-2; the other terminal of the ribbon cable is the DB 9-Pin female socket which matches the DB 9-Pin male plug of the cable. On the other terminal of the DB 9-Pin male plug of the cable is connected to the DB 9-Pin female socket of the IMP-ARIO/IMP-ARIO64. For more detailed descriptions, please refer to Fig. 1-5 and Fig. 1-6.

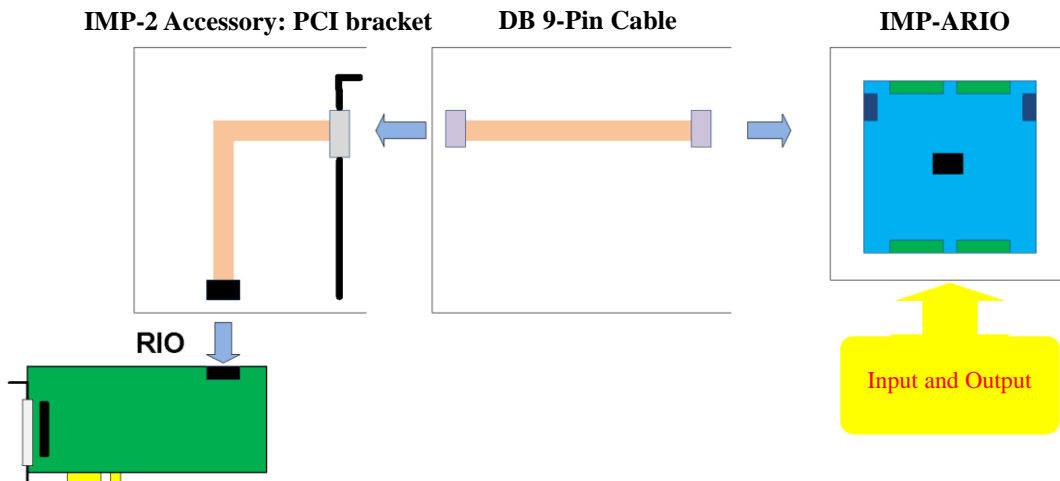


Fig.1-4 The connection between IMP-2 and IMP-ARIO

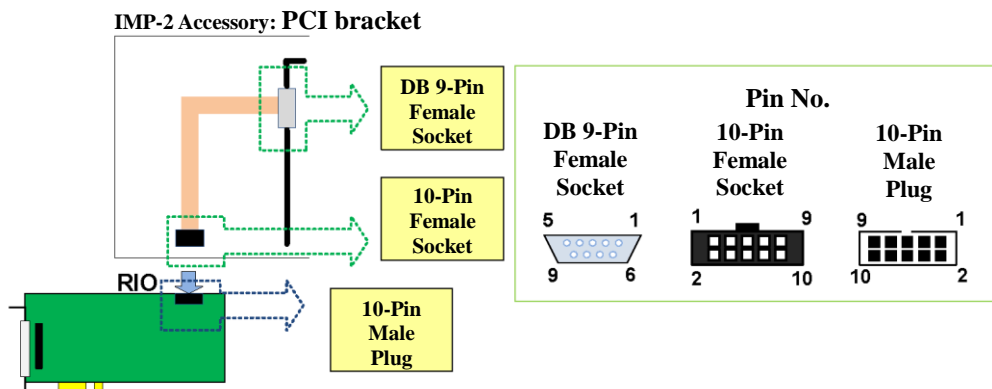


Fig. 1-5 Description of PCI bracket

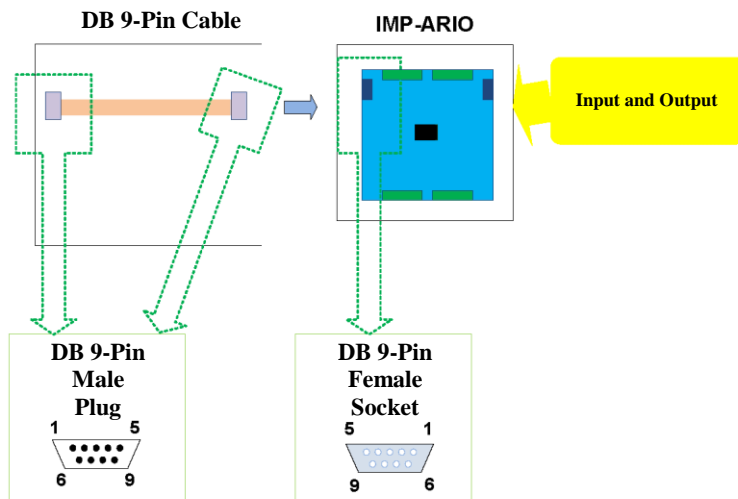


Fig. 1-6 The DB 9-Pin cable and the connector on the IMP-ARIO

Chapter 2 Hardware Installation

2.1 IMP-ARIO Hardware Installation

2.1.1 Layout of the IMP-ARIO Hardware

The diagram of the I/O pins on the IMP-ARIO is shown in Fig. 2-1, where the OUT0~OUT15 are mapped to output 0 to 15 and the IN0~IN15 are mapped to input 0 to 15. The COM is supplied with a voltage at 5~24V or 0V for the input. The 5V/GND (CN3) is used for 5V input. The female sockets (TR_1, TR_2) for communications are DB 9-Pin female sockets, in which the TR_1 is used for connecting the IMP-2, the IMP-ARIO or the IMP-ARIO64 in the previous stage and the TR_2 is used for connecting the IMP-ARIO or the IMP-ARIO64 in the next stage.

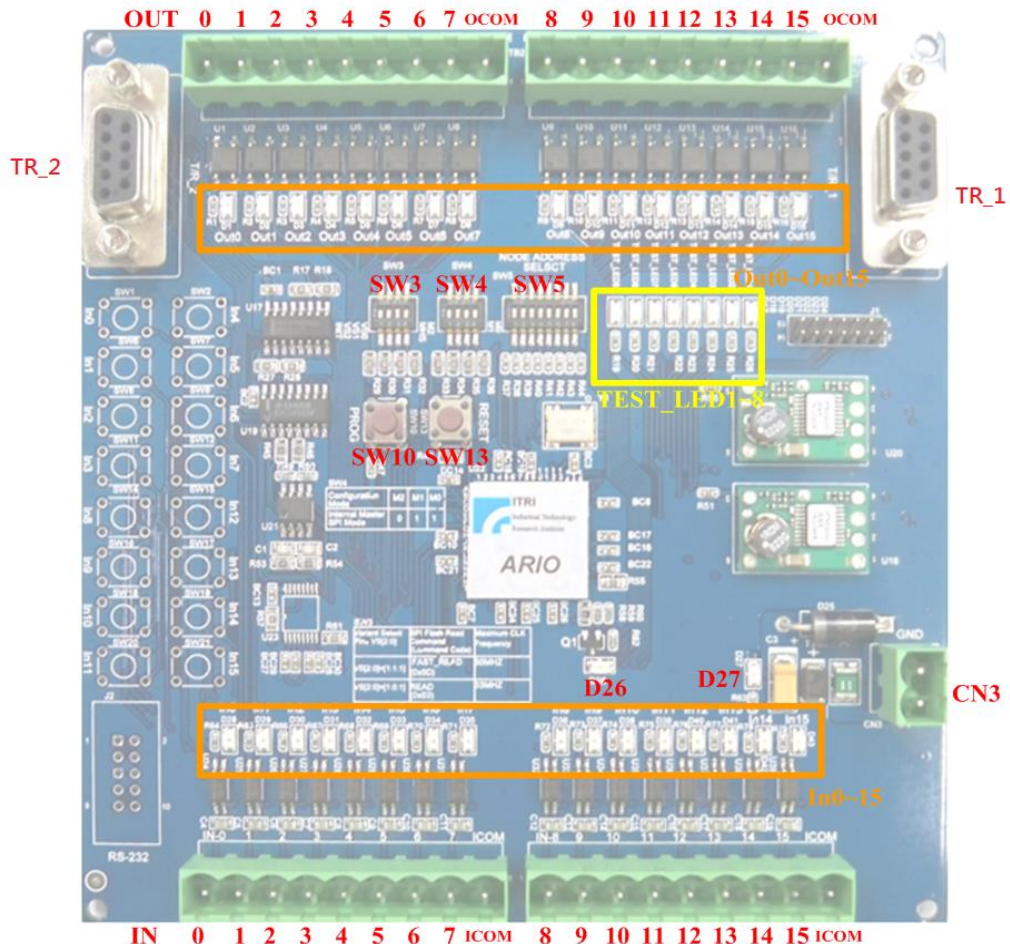


Fig. 2-1 The I/O pins on the IMP-ARIO

2.1.2 IMP-ARIO Pin Assignments of Connectors

For TR_1 and TR_2 communication connectors, the pin assignments are as follows:

Pin	Function	Assignment
1	N.C.	For future expansion
2	N.C.	For future expansion
3	TX-	Serial data differential output signal
4	RX-	Serial data differential input signal
5	GND	Ground
6	N.C.	For future expansion
7	N.C.	For future expansion
8	TX+	Serial data differential output signal
9	RX+	Serial data differential input signal

For CN3 power connector, the pin assignments are as follows:

Pin	Function	Assignment
1	GND	Ground
2	5V	Power

2.1.3 IMP-ARIO Indicator Definition

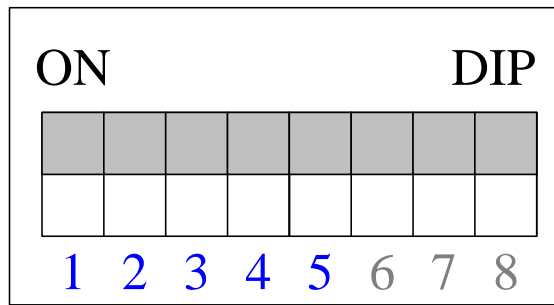
The definitions of the LED indicators on the IMP-ARIO are as follows:

Location	Color	Function
D1	Red	Out0 indicator
D2	Red	Out1 indicator
D3	Red	Out2 indicator
D4	Red	Out3 indicator
D5	Red	Out4 indicator
D6	Red	Out5 indicator
D7	Red	Out6 indicator
D8	Red	Out7 indicator
D9	Red	Out8 indicator
D10	Red	Out9 indicator
D11	Red	Out10 indicator
D12	Red	Out11 indicator
D13	Red	Out12 indicator
D14	Red	Out13 indicator
D15	Red	Out14 indicator
D16	Red	Out15 indicator

D26	Red	Firmware completion indicator
D27	Red	Power indicator
D28	Green	In0 indicator
D29	Green	In1 indicator
D30	Green	In2 indicator
D31	Green	In3 indicator
D32	Green	In4 indicator
D33	Green	In5 indicator
D34	Green	In6 indicator
D35	Green	In7 indicator
D36	Green	In8 indicator
D37	Green	In9 indicator
D38	Green	In10 indicator
D39	Green	In11 indicator
D40	Green	In12 indicator
D41	Green	In13 indicator
D42	Green	In14 indicator
D43	Green	In15 indicator
TEST_LED1	Red	Reserved indicator
TEST_LED2	Red	Reserved indicator
TEST_LED3	Red	Reserved indicator
TEST_LED4	Red	Reserved indicator
TEST_LED5	Red	Reserved indicator
TEST_LED6	Red	Reserved indicator
TEST_LED7	Red	Reserved indicator
TEST_LED8	Red	Watchdog indicator <ul style="list-style-type: none"> ● Light Off: Watchdog disabled ● Light On: Watchdog enabled and connected ● Flashing Light: Watchdog enabled and disconnected

2.1.4 IMP-ARIO Address Select

SW5 (NODE ADDRESS SELECT) DIP1~DIP5 can be configured by the IMP-ARIO addresses 0~31. In a system, up to 32 IMP-ARIO can be serially connected. However, one address can only be used to identify a single IMP-ARIO; if 32 IMP-ARIO are serially connected, they must be configured with distinct addresses. The diagram of SW5 settings is as shown in Fig. 2-2 below, and the configuration method is as shown in Fig. 2-3 below.



(SW5)

Fig. 2-2 SW5 settings

DIP Switch Setting	NODE ADDRESS	DIP Switch Setting	NODE ADDRESS	DIP Switch Setting	NODE ADDRESS	DIP Switch Setting	NODE ADDRESS
	0		8		16		24
	1		9		17		25
	2		10		18		26
	3		11		19		27
	4		12		20		28
	5		13		21		29
	6		14		22		30
	7		15		23		31

Fig. 2-3 Slave node address setting

2.1.5 IMP-ARIO Button and Switch Settings

The functions of various switches are described below:

SW	Definition	Description of Settings
SW3	SPI Boot ROM selection	Fig.2-4
SW4	Hardware boot mode setting	Fig.2-4
SW5: DIP1~5	Slave node address setting	Fig.2-3
SW5: DIP6~7	Transfer rate setting	Fig.2-6
SW5: DIP8	Watchdog function setting	Fig.2-7

SW10	Hardware reset (PROG)	X
SW13	System reset (RESET)	X

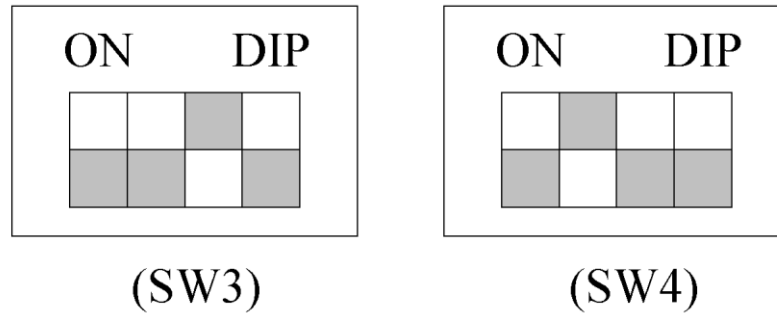


Fig. 2-4 Diagram of SW3 and SW4 settings

The diagram of SW3 and SW4 settings is shown in Fig. 2-4, where the SW3 is used for SPI Boot ROM selection and SW4 is used for hardware boot mode setting. The setting must be identical to that shown in Fig. 2-4 to ensure normal operation of the system.

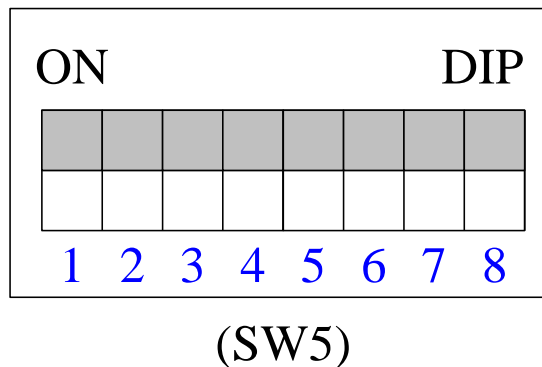


Fig. 2-5 Diagram of SW5 settings

The diagram of the SW5 settings is shown in Fig. 2-5, where the switches are arranged from left to right as DIP1~DIP8. The description for the function of each DIP switch is as follows.

- DIP1~5: The slave station address select (NODE ADDRESS SELECT) can be configured by the IMP-ARIO addresses 0~31. The configuration method is as shown in 2.1.4.
- DIP6~7: Transfer rate setting. The default transfer rate between the IMP-ARIO and the IMP-2 is 0.195MHz. The user can change the transfer rate by using the DIP switch SW5 (DIP6~7). Note that after setting, pressing the SW10 to apply a new setting, and the new setting value must be identical to that in the IMP-2; otherwise, it may lead to the transmission failure. For this setting, please refer to Fig. 2-6.

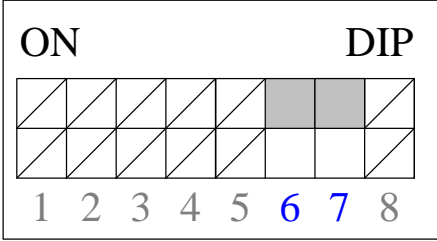
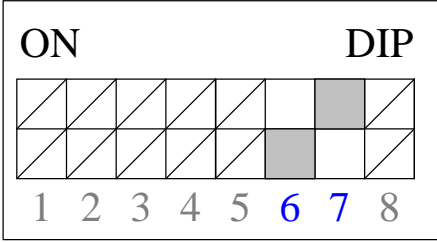
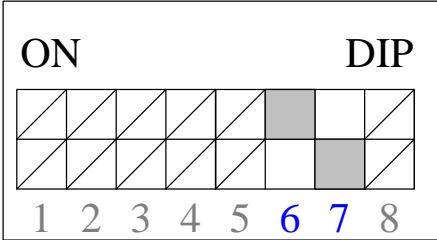
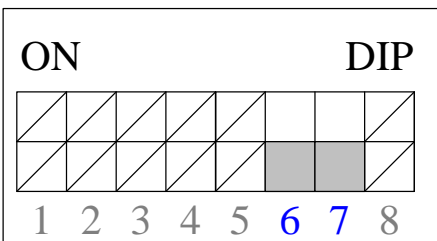
DIP Switch Settings	Clock divider	Transfer Rate
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	255	0.195MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	100	0.5MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	50	1MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	25	2MHz

Fig. 2-6 Transfer rate settings

- **DIP8:** Watchdog function setting. The watchdog function is enabled in the default setting. When the connection with the IMP-2 is disconnected, it will force all the outputs to be the default one (zero output); if this function is turned off, when the connection with the IMP-2 is disconnected, the output states will remain in the state before the connection is disconnected. The SW5 (DIP8) can be used to configure the watchdog function. For details of this setting, please refer to Fig. 2-7.

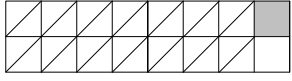
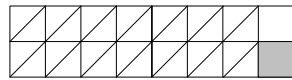
DIP Switch Setting	Watchdog Function Setting
<p data-bbox="555 387 603 416">ON</p> <p data-bbox="794 387 842 416">DIP</p>  <p data-bbox="571 506 831 535">1 2 3 4 5 6 7 8</p>	<p data-bbox="970 456 1059 486">Enable</p>
<p data-bbox="555 611 603 640">ON</p> <p data-bbox="794 611 842 640">DIP</p>  <p data-bbox="571 723 831 752">1 2 3 4 5 6 7 8</p>	<p data-bbox="978 674 1074 703">Disable</p>

Fig. 2-7 Watchdog function setting

2.2 IMP-ARIO64 Hardware Installation

2.2.1 Layout of the IMP-ARIO64 Hardware

The diagram of the I/O pins on the IMP-ARIO64 is shown in Fig. 2-8, where the OUT0~OUT31 are mapped to output 0 to 31 and the IN0~IN31 are mapped to input 0 to 31. The COM is supplied with a voltage at 5~24V or 0V for the input. The 5V/GND (CN1) is used for 5V input. The female sockets (TR_1, TR_2) for communications are DB 9-Pin female sockets, in which the TR_1 is used for connecting the IMP-2, the IMP-ARIO or the IMP-ARIO64 in the previous stage and the TR_2 is used for connecting the IMP-ARIO or the IMP-ARIO64 in the next stage.

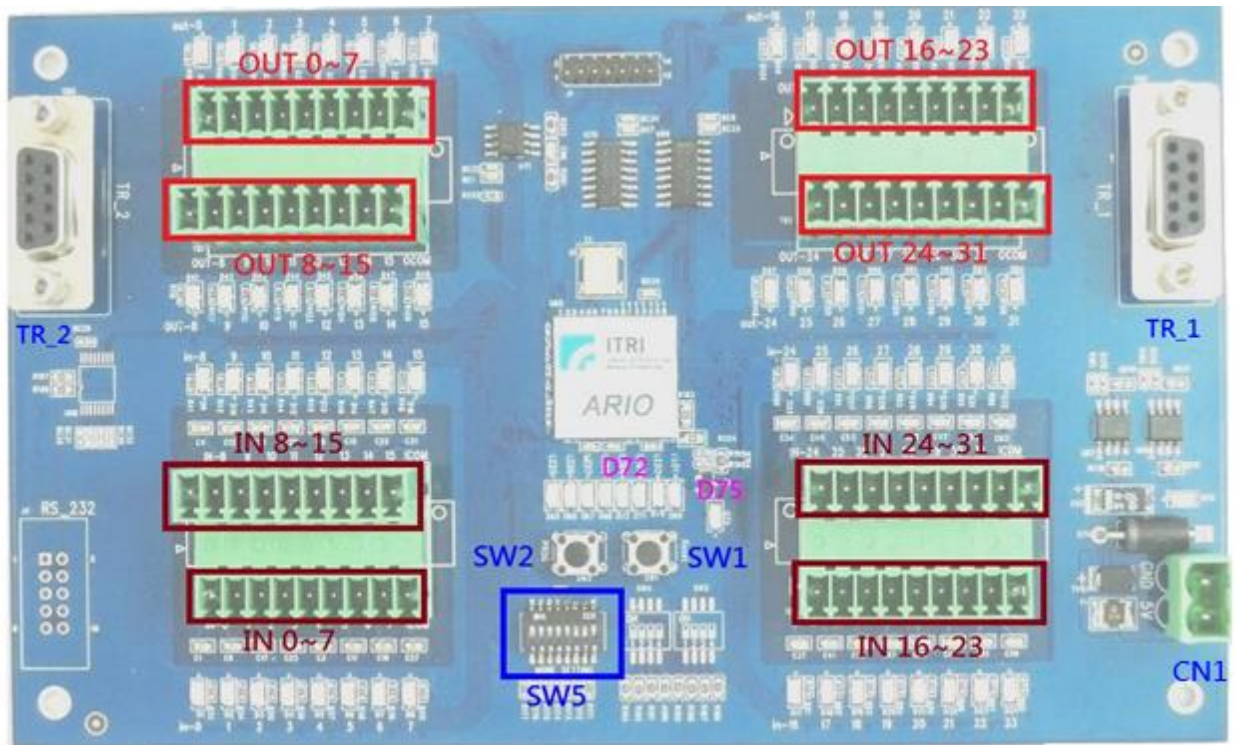


Fig. 2-8 The I/O pins on the IMP-ARIO64

2.2.2 IMP-ARIO64 Pin Assignments of Connectors

For TR_1 and TR_2 communication connectors, the pin assignments are as follows:

Pin	Function	Assignment
1	N.C.	For future expansion
2	N.C.	For future expansion
3	TX-	Serial data differential output signal
4	RX-	Serial data differential input signal
5	GND	Ground
6	N.C.	For future expansion
7	N.C.	For future expansion
8	TX+	Serial data differential output signal
9	RX+	Serial data differential input signal

For CN1 power connector, the pin assignments are as follows:

Pin	Function	Assignment
1	GND	Ground
2	5V	Power

2.2.3 IMP-ARIO64 Indicator Definition

The definitions of the LED indicators on the IMP-ARIO64 are as follows:

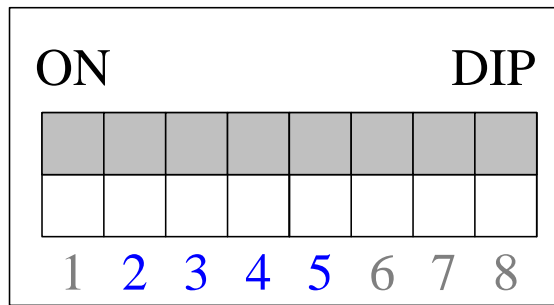
Location	Color	Function
D1	Green	In0 indicator
D2	Green	In1 indicator
D3	Green	In2 indicator
D4	Green	In3 indicator
D5	Green	In4 indicator
D6	Green	In5 indicator
D7	Green	In6 indicator
D8	Green	In7 indicator
D9	Green	In8 indicator
D10	Green	In9 indicator
D11	Green	In10 indicator
D12	Green	In11 indicator
D13	Green	In12 indicator
D14	Green	In13 indicator
D15	Green	In14 indicator
D16	Green	In15 indicator

D17	Green	In16 indicator
D18	Green	In17 indicator
D19	Green	In18 indicator
D20	Green	In19 indicator
D21	Green	In20 indicator
D22	Green	In21 indicator
D23	Green	In22 indicator
D24	Green	In23 indicator
D25	Green	In24 indicator
D26	Green	In25 indicator
D27	Green	In26 indicator
D28	Green	In27 indicator
D29	Green	In28 indicator
D30	Green	In29 indicator
D31	Green	In30 indicator
D32	Green	In31 indicator
D33	Red	Out0 indicator
D34	Red	Out1 indicator
D35	Red	Out2 indicator
D36	Red	Out3 indicator
D37	Red	Out4 indicator
D38	Red	Out5 indicator
D39	Red	Out6 indicator
D40	Red	Out7 indicator
D41	Red	Out8 indicator
D42	Red	Out9 indicator
D43	Red	Out10 indicator
D44	Red	Out11 indicator
D45	Red	Out12 indicator
D46	Red	Out13 indicator
D47	Red	Out14 indicator
D48	Red	Out15 indicator
D49	Red	Out16 indicator
D50	Red	Out17 indicator
D51	Red	Out18 indicator
D52	Red	Out19 indicator
D53	Red	Out20 indicator
D54	Red	Out21 indicator
D55	Red	Out22 indicator
D56	Red	Out23 indicator
D57	Red	Out24 indicator

D58	Red	Out25 indicator
D59	Red	Out26 indicator
D60	Red	Out27 indicator
D61	Red	Out28 indicator
D62	Red	Out29 indicator
D63	Red	Out30 indicator
D64	Red	Out31 indicator
D65	Red	Reserved indicator
D66	Red	Reserved indicator
D67	Red	Reserved indicator
D68	Red	Reserved indicator
D69	Red	Reserved indicator
D70	Red	Reserved indicator
D71	Red	Reserved indicator
D72	Red	Watchdog indicator <ul style="list-style-type: none"> ● Light Off: Watchdog disabled ● Light On: Watchdog enabled and connected ● Flashing Light: Watchdog enabled and disconnected
D73	Red	Power indicator
D75	Red	Firmware completion indicator

2.2.4 IMP-ARIO64 Address Select

SW5 (NODE ADDRESS SELECT) DIP2~DIP5 can be configured by IMP-ARIO64 addresses 0~31. In a system, up to 16 IMP-ARIO64 can be serially connected. However, one address can only be used once; if 16 IMP-ARIO64 are serially connected, they must be configured with distinct addresses. The diagram of SW5 settings is as shown in Fig. 2-9 below, and the configuration method is as shown in Fig. 2-10 below.



(SW5)

Fig. 2-9 SW5 settings

DIP Switch Setting	IN/OUT 0~15 Address	IN/OUT 16~31 Address	DIP Switch Setting	IN/OUT 0~15 Address	IN/OUT 16~31 Address
	0	1		16	17
	2	3		18	19
	4	5		20	21
	6	7		22	23
	8	9		24	25
	10	11		26	27
	12	13		28	29
	14	15		30	31

Fig. 2-10 Slave node address setting

2.2.5 IMP-ARIO64 Button and Switch Settings

The functions of various switches are described below:

SW	Definition	Description of Settings
SW1	System reset (RESET)	X
SW2	Hardware reset (PROG)	X
SW5: DIP1	N.C.	X
SW5: DIP2~5	Slave node address setting	Fig.2-10
SW5: DIP6~7	Transfer rate setting	Fig.2-12
SW5: DIP8	Watchdog function setting	Fig.2-13

The diagram of the SW5 settings is shown in Fig. 2-11, where the switches are arranged from left to right as DIP1~DIP8. The description for the function of each DIP switch is as follows.

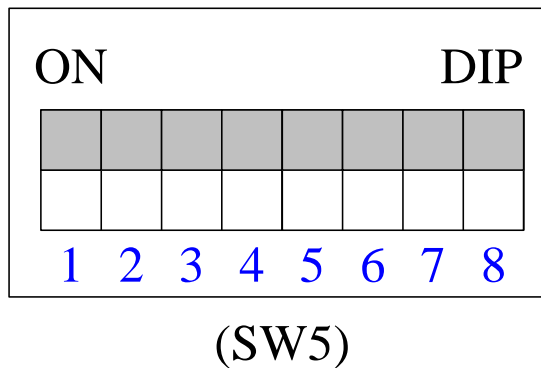


Fig. 2-11 Diagram of SW5 settings

- DIP1: Reserved, for future expansion.
- DIP2~5: The slave station address select (NODE ADDRESS SELECT) can be configured by the IMP-ARIO64 addresses 0~31. A single IMP-ARIO64 has two addresses, and the configuration method is as shown in 2.2.4.
- DIP6~7: Transfer rate setting. The default transfer rate between the IMP-ARIO64 and the IMP-2 is 0.195MHz. The user can change the transfer rate by using the DIP switch SW5 (DIP6~7). Note that after setting, pressing the SW2 to apply a new setting, and the new setting value must be identical to that in the IMP-2; otherwise, it may lead to the transmission failure. For this setting, please refer to Fig. 2-12.

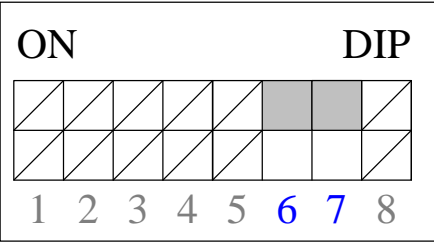
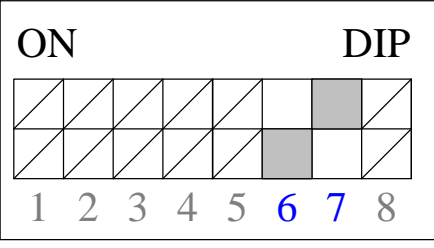
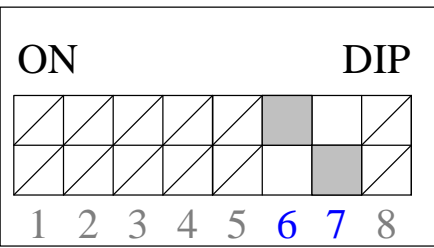
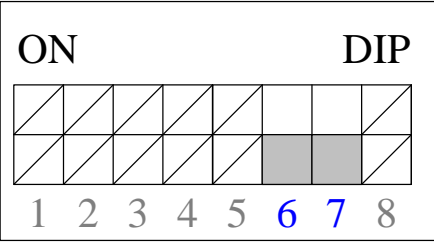
DIP Switch Settings	Clock divider	Transfer Rate
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	255	0.195MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	100	0.5MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	50	1MHz
 <p>ON DIP</p> <p>1 2 3 4 5 6 7 8</p>	25	2MHz

Fig. 2-12 Transfer rate settings

- **DIP8:** Watchdog function setting. The watchdog function is enabled in the default setting. When the connection with IMP-2 is disconnected, it will force all the outputs to be the default one (zero output); if this function is turned off, when the connection with the IMP-2 is disconnected, the output states will remain in the state before the connection is disconnected. The SW5 (DIP8) can be used to configure the watchdog function. For details of this setting, please refer to Fig. 2-13.

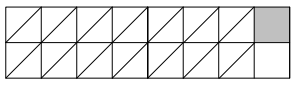

DIP Switch Setting	Watchdog Function Setting
<p>ON DIP</p>  <p>1 2 3 4 5 6 7 8</p>	<p>Enable</p>
<p>ON DIP</p>  <p>1 2 3 4 5 6 7 8</p>	<p>Disable</p>

Fig. 2-13 Watchdog function setting

Chapter 3 System Wiring and Mechanical Dimensions

3.1 Output Wiring

Sink or Source output type is provided to connect the output connections to solenoid valves or Relay application.

3.1.1 Source Output Type

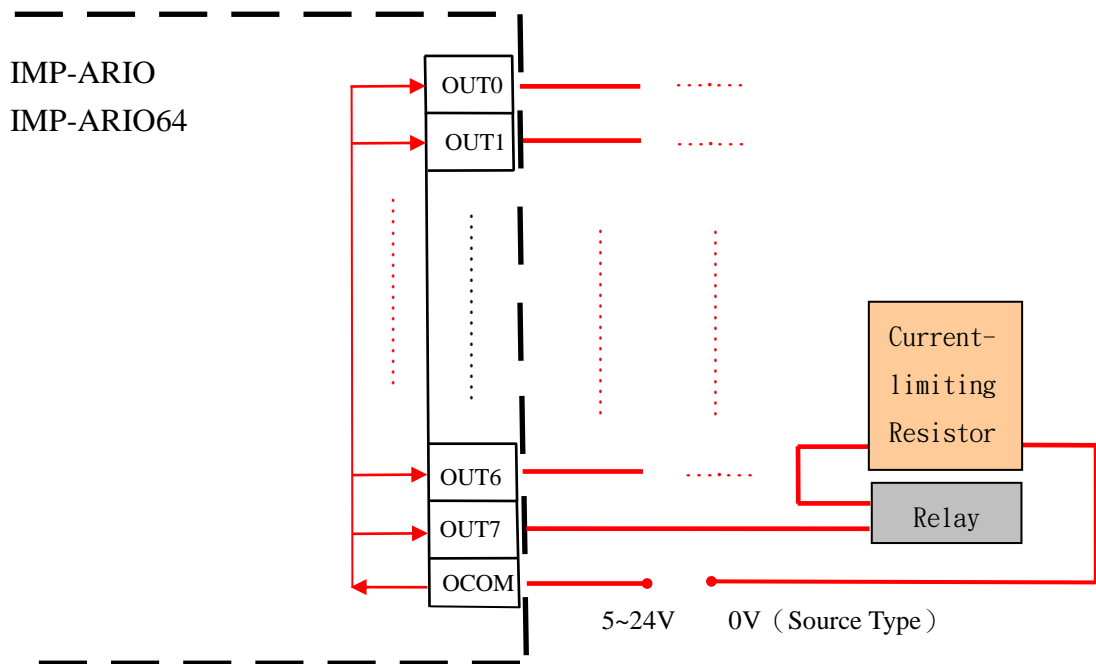


Fig. 3-1 Source output type wiring diagram

The source output type wiring diagram is shown in Fig. 3-1. When OCOM is connected with a voltage input at 5~24V, it operates in source-output type. When one terminal of the load Relay solenoid connects to output connection (ex. OUT7), the other terminal connects the current limiting resistor to 0V. When the output is at 1, the Relay is ON and current flows from the output connection.

3.1.2 Sink Type Output

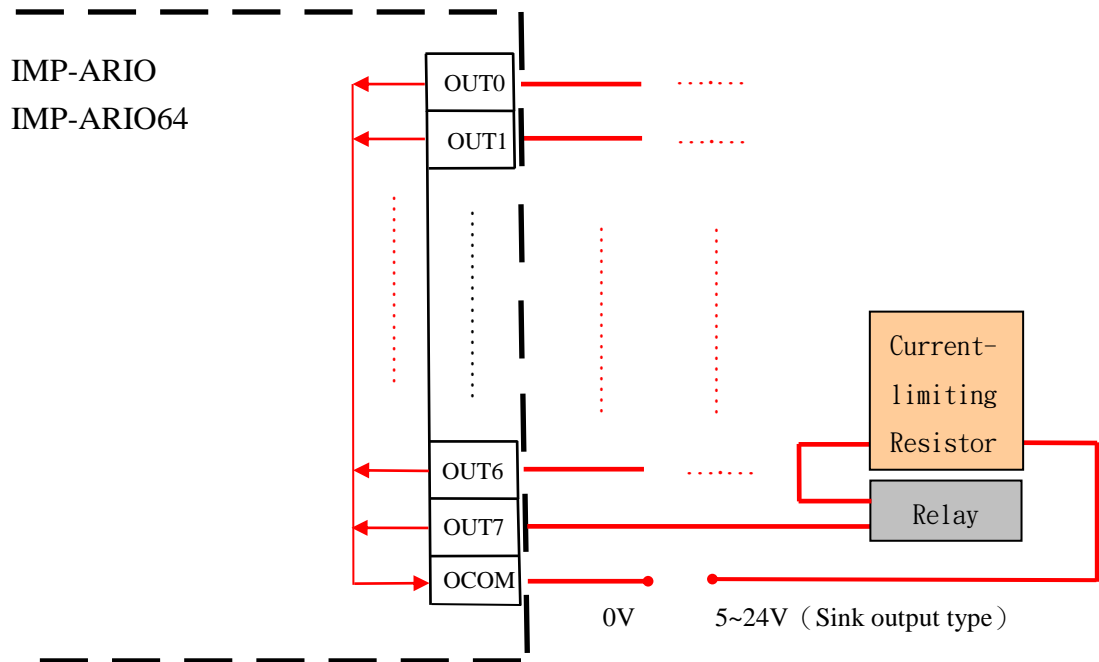


Fig. 3-2 Sink output type wiring diagram

The sink type wiring diagram is shown in Fig. 3-2. When OCOM is connected with a voltage input at 0V, it operates in sink-output type. When one terminal of the load Relay solenoid connects to output connection (ex. OUT7), the other terminal connects the current limiting resistor to 5~24V. When the output is at 1, the Relay is ON and current flows into the output connection.

3.2 Input Wiring

Sink or Source input type is provided to connect the input connections.

3.2.1 Source Input Type

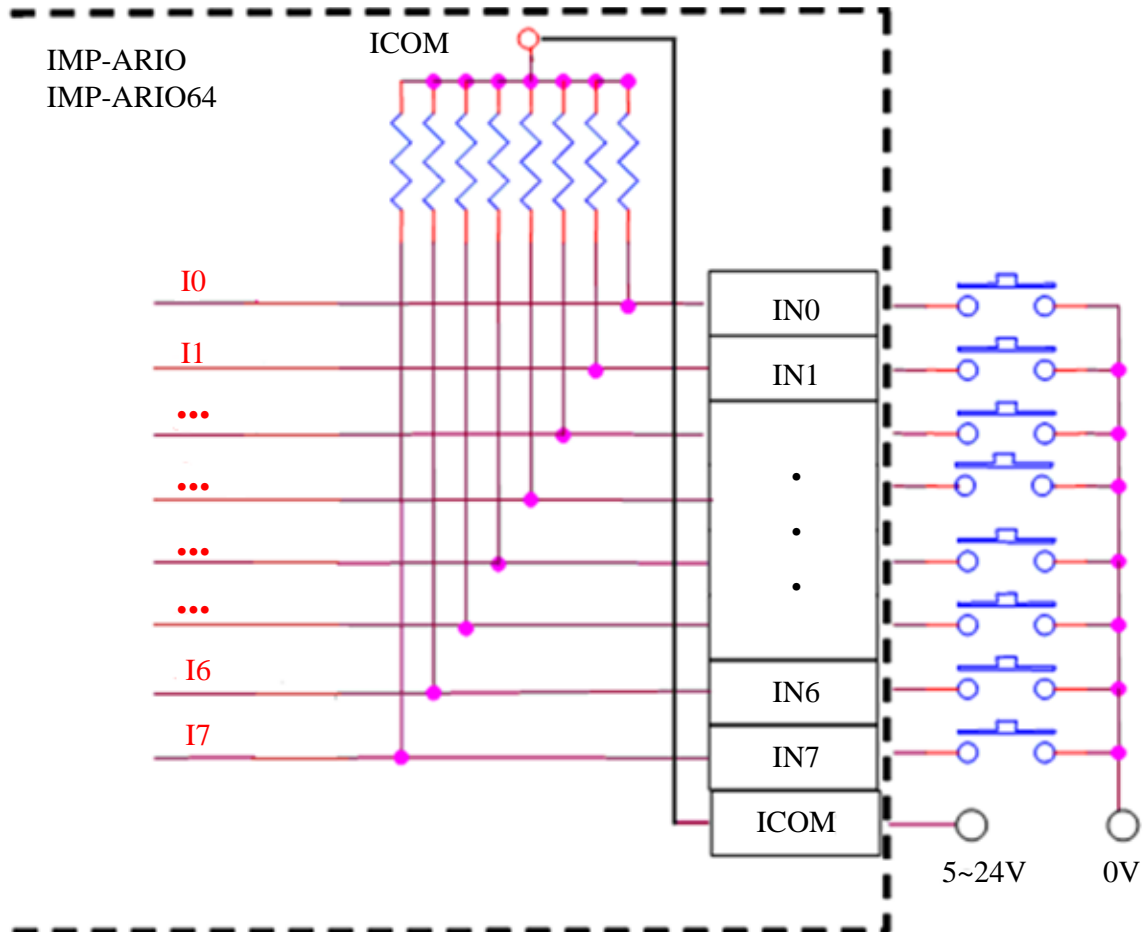


Fig. 3-3 Source-input type contact wiring

The wiring diagram of the source input type is shown in Fig. 3-3. When ICOM is connected to 5~24V, it operates in source-input type and the current flows from the input connections. When one terminal of the input device (for example: Switch Button) is connected to input (for example: I0) and the other terminal is connected to 0V. When the switch is turned on (for example: pressing the Switch Button), the state of the ARIIO input becomes 0; otherwise the state reads 1.

3.2.2 Sink Input Type

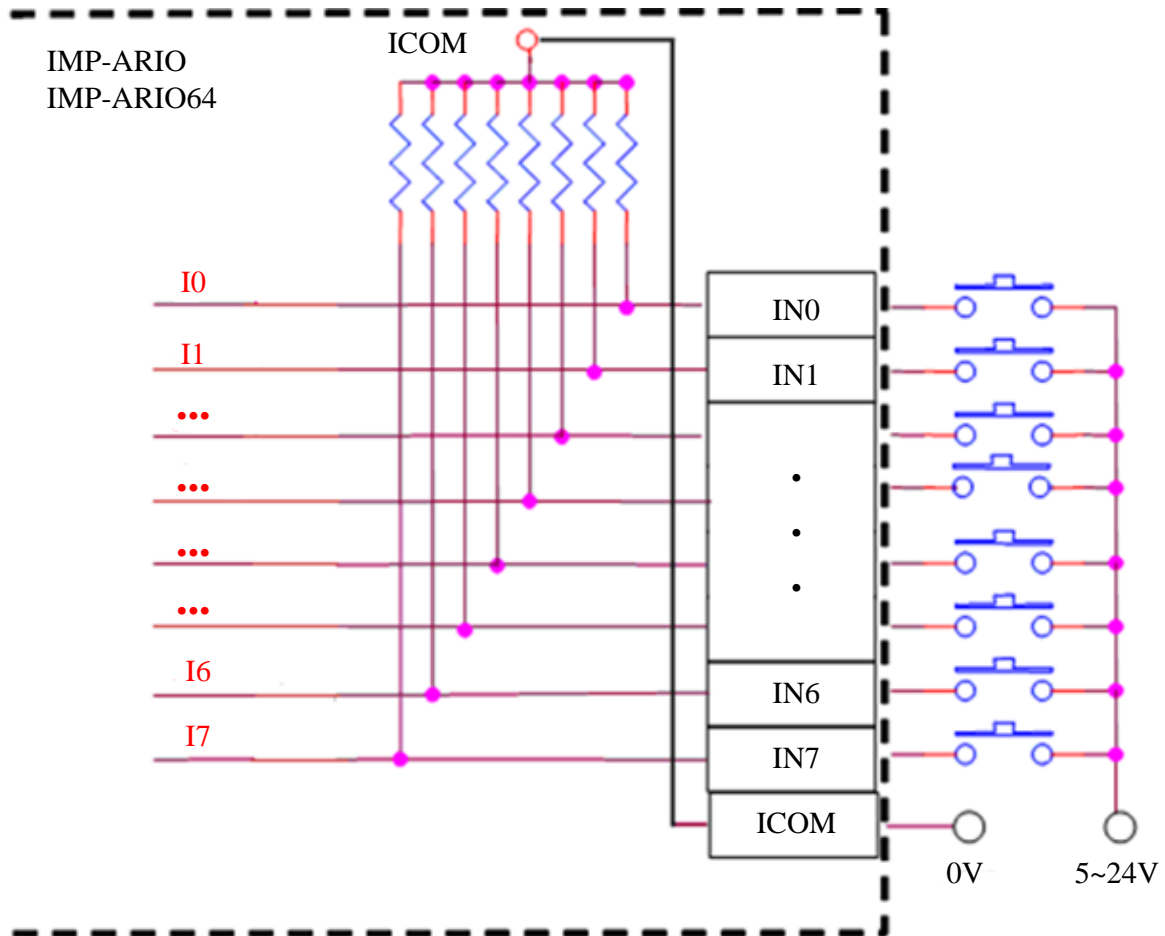
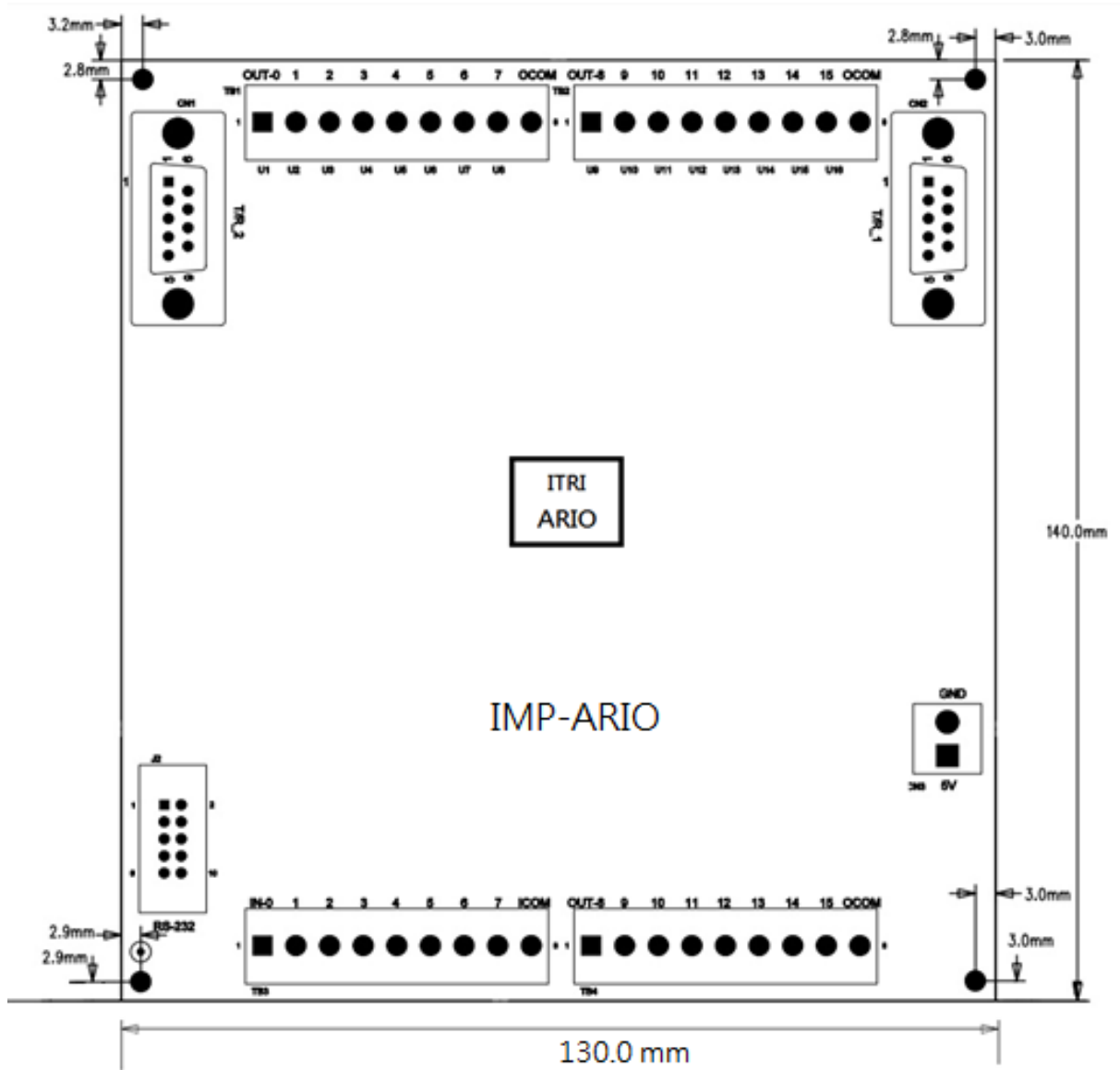


Fig. 3-4 Sink-input type contact wiring

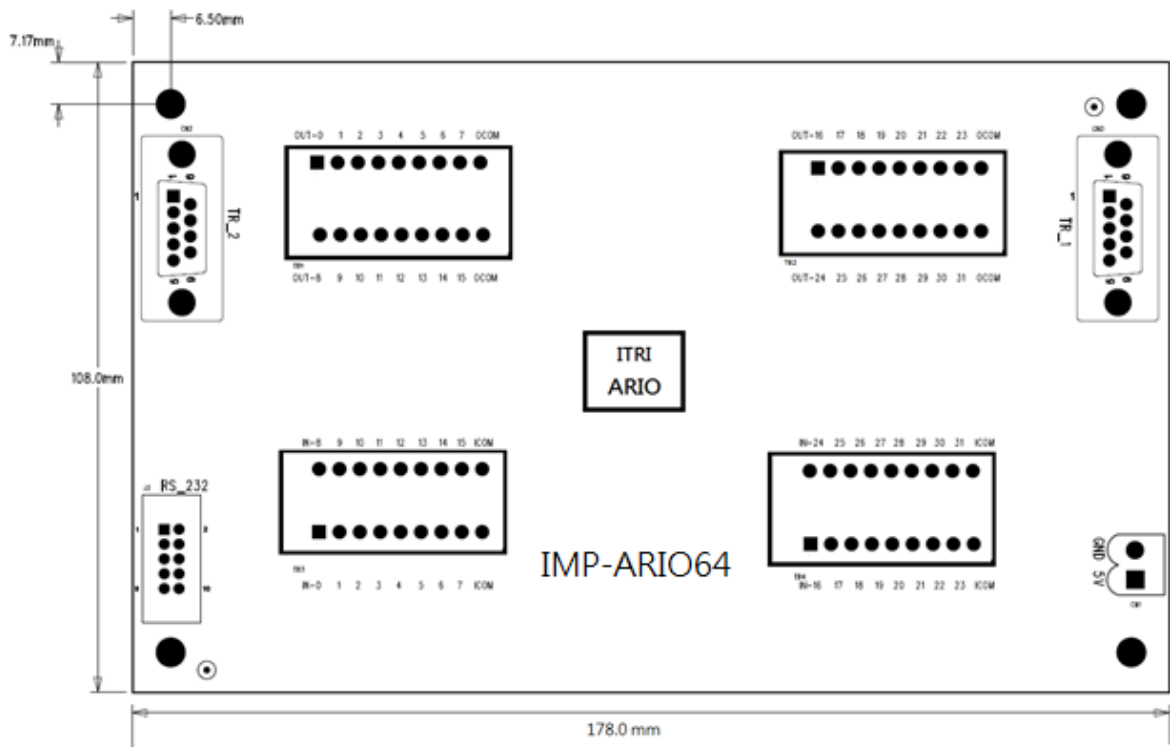
The wiring diagram of the sink input type is shown in Fig. 3-4. When ICOM is connected to 0V, it operates in sink-input type and the current flows into the input connections. When one terminal of the input device (for example: Switch Button) is connected to input (for example: I0) and the other terminal is connected to 5~24V. When the switch is turned on (for example: pressing the Switch Button), the state of the ARIO input becomes 0; otherwise the state reads 1.

3.3 Mechanical Dimensions



Note: Screw size is 3.0 mm.

Fig. 3-5 Mechanical dimensions of IMP-ARIO



Note: Screw size is 3.0 mm.

Fig. 3-6 Mechanical dimensions of IMP-ARIO64

Revision History

Date	Rev.	Revised contents
2014.03	V1.0.0	IMP-ARIO/IMP-ARIO64 hardware user manual was added